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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,512	04/02/2001	Koutaro Hachiya	Q63926	7509

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,512	HACHIYA, KOUTARO	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *10/27/2005*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been presented for examination based on applicant's amendment 17 August 2005. Claims 1-16 remain rejected by the examiner.

Response to Arguments

2. Applicant's arguments filed 17 August 2005 have been fully considered.

Regarding applicant's response to IDS objection: The examiner withdraws the IDS objection n view of applicants IDS submission of "Matrix Calculation Software", Dr. T. Kokuni, Maruzen, filed 17 August 2005.

Regarding applicant's response to 101 rejection: The examiner withdraws the 101 rejection in view of applicant's amendment to the claims filed 17 August 2005.

Regarding applicant's response to 112(1) rejection: In evaluating the enablement issues relating to the "determinator" and "replacer" the examiner applied the factors as set forth in In re Wands. In re Wands (CA FC) 8 USPQ2d 1400, 1404 (9/30/1998) provides an 8 factor test for determining undue experimentation (MPEP 2164.01(a), factors (A) to (H)). Also see White Consolidated Industries, Inc. v. Vega Servo-Control Inc. (CAFC) 218 USPQ 961, 963 (7/25/83). Here the examiner determined several reasons for establishing a reasonable basis to question the enablement (MPEP 2164.04) of the "determinator" and "replacer" based on application of the undue experimentation factors (MPEP 2164.01(a), factors (A) to (H)). First, and as noted in the office action (page 7), the specification provided no description (algorithms, techniques, etc.) describing specifically how a skilled artisan would actually implement

the claimed "determinator" and "replacer". That is, the amount of direction provided to a skilled artisan (factor (F)) appears inconsistent with what which was required by the state of the prior art (factor (C)). Note that prior art Garg (background), for example, specifically address to problem of the complexity (difficulty) involved in attaining high performance in matrix computations. (i.e. factors (B), (C), and (E)) Second, the specification provided no clear definition of the terms "determinator" and "replacer" or how they were to be applied to the reordering of the matrix. Hence, the examiner determined that the quantity of experimentation (factor (H)) required by a skilled artisan to implement the claimed limitations (factor (A)) was relatively high when compared to the state of the prior art. A reasonable basis to question enablement therefore appears to be satisfied according to MPEP 2164.04. MPEP 2164(a) Undue Experimentation Factors further recites:

> *"A conclusion of lack of enablement means that, based on the evidence regarding each of the above factors, the specification, at the time the application was filed, would not have taught one skilled in the art how to make and/or use the full scope of the claimed invention without undue experimentation. In re Wright, 999 F.2d 1557,1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993)."*

Therefore, when weighing the Wands factors, the examiner determined that based on the evidence regarding each of the undue experimentation factors, one skilled in the art would not know how to make and/or use the claimed subject matter from the description contained in the specification without undue experimentation.

ENABLEMENT BURDEN AND STANDARD. The "initial burden to establish a reasonable basis to question the enablement provided for the claimed invention" appears to be satisfied, according to MPEP 2164.04. Specifically, In re Marzochi, 439 F.2df 220, 224, 169 USPQ 367, 370 (CCPA 1971) states "it is incumbent upon the

Patent Office, whenever a rejection on this basis [enablement] is made, explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement". Here, the Examiner has presented some broad evidence (i.e. the terms "determinator" and "replacer" do not appear in the specification) and related specific technical reasons (see: office action page 7, paragraph 2) that clearly establish "a reasonable basis to question the enablement".

Thus, the burden should now be shifted to the Applicant to "present persuasive arguments, supported by suitable proofs where necessary", according to MPEP § 2164.05. However, applicants have merely referenced vague specification sections (page 7, lines 13-15, 18-20) and stated that a skilled artisan could somehow realize the "determinator" and "replacer" from passages that merely recite, "the system inputs the circuit description…", and "the above method … is actualized by a computer program." These passages clearly do not provide sufficient guidance (direction) to a skilled artisan such that the "determinator" and "replacer" could be implemented by computer program. The examiner therefore maintains the 112(1) rejection. However, the examiner suggests that amending claims to recite a "determining means for.." (instead of a "determinator") and a replacing means for.." (instead of a "replacer") would resolve this issue. (See: Interview Summary, 10/27/2005)

Regarding applicant's response to 103(a) rejection: The thrust of applicants arguments appear to center around arguing that the prior art (Garg) does not disclose determining the number of non-zero elements. The examiner first notes that applicants

appear to admit that Garg does in fact determine the number of non-zero elements at least in order to perform the factorization where the number of zero elements being replaced by non-zero elements is reduced (Garg 533-37). Obviously, a knowledge of the non-zero elements would be available (i.e. known) in the factorization process given that the zero elements are being replaced by non-zero elements. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicants also argue that there is no teaching of determining a combination of rows and columns based on a length of the critical path but critical path length limitations are not specifically recited in the rejection claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The examiner therefore maintains the 103(a) rejection.

The examiner suggests that applicants contact the examiner to conduct an interview in order to resolve the issues outlined in this office action. (See: Interview Summary, 10/27/2005)

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 5, 6, 11, and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. *The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*

Specifically, apparatus claims 5, 6, 11, and 12 recite limitations relating to a "determinator" and a "replacer" whose structural elements (features) have not been disclosed in Figures 1-17, and, the examiner has found no teaching in applicant's specification that specifically discloses the operation of the "determinator" or the "replacer". In fact, the terms "determinator" and "replacer" do not appear to be present in the disclosure at all. Further, the specification provides no clear description (algorithms, techniques, etc.) sufficient to allow skilled artisan to actually implement the claimed subject matter. Accordingly, a skilled artisan would not be able to make and/or use the claimed invention's "determinator" and "replacer" from the description contained in applicant's specification. Applicant's preliminary amendment filed on 31 May 2001 and the proposed drawing changes filed 31 January 2001 merely labeling blocks S202 and S203 of Figure 1 with the terms "determinator" and "replacer" does not cure this deficiency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,601,080 issued to Garg in view of "On Efficient Band Matrix Arithmetic", W. Eberly, IEEE 0-8186-2900-2/92, IEEE 1992.

Independent claims 1,2, 5-8, and 11-13 are drawn to:

> method and apparatus for reordering elements of a coefficient matrix representing linear simultaneous equations produced by parallel processing using Gaussian elimination by steps of:
>
> - based on number of non-zero elements in coefficient matrix and accumulative processing time (lengths of critical paths) of Gaussian elimination of coefficient matrix, determining (determinator: claims 5,6,11,12) a first/second combination of row and column from the coefficient matrix
>
> - performing replacement (replacer: claims 5,6,11,12) of elements between first/second combination of row and column within the coefficient matrix. (claim13: selecting/replacing pivots in the coefficient matrix)

Regarding dependent claims 1,2, 5-8, and 11-13: As outlined above, this group of independent claims includes the same limitations relating to a method, apparatus, and circuit simulation method for reordering the elements of a coefficient matrix representing linear simultaneous equations. These limitations are rendered obvious in view of the

teachings of U.S. Patent 6,601,080 issued to Garg in view of U.S. Patent 6,144,932 issued to Hachiya. Garg discloses the elements of the claimed limitations of the present invention as follows:

- method and apparatus for reordering elements of a coefficient matrix representing linear simultaneous equations produced by parallel processing using Gaussian elimination: Garg discloses reordering to the elements of a coefficient matrix (Abstract, CL5-L29-37, Fig. 2) that represent linear simultaneous equations (Summary, CL1-L17, CL3-L1-5, CL9-L49) and the use of Gaussian elimination (CL5-L53).

- based on number of non-zero elements in coefficient matrix and accumulative processing time (lengths of critical paths) of Gaussian elimination of coefficient matrix, determining (determiner) a first/second combination of row and column from the coefficient matrix: Garg discloses determining the number of non-zero elements in the coefficient matrix (Abstract, CL3-L5, CL5-L39) for further determining combinations of rows and columns from the coefficient matrix (CL6-L20-40, Fig. 4). Garg also discloses the use of Gaussian elimination (CL5-L53) as noted above.

- performing replacement (replacer) of elements between first/second combination of row and column within the coefficient matrix. Garg discloses the replacement (substitution) and reordering of elements (CL1-L30, CL5-L29-35, Fig. 2) between multiple (1st, 2nd, etc.) combinations of rows and columns (CL6-L20-59, Fig. 4) within the coefficient matrix (Abstract, CL3-L2)

Garg does not explicitly disclose considering the accumulative processing time or length of critical paths.

Eberly discloses simulating the operation of an electronic circuit by parallel processing and using a coefficient matrix for solving simultaneous linear equations. In particular, Hachiya discloses these elements while also considering the accumulative parallel processing time and the length of critical paths. (Abstract, Sections) Eberly discloses the elements of the claimed limitations of the present invention as follows:

- *accumulative processing time: Eberly considers the critical path execution time (processing time required) in parallel processing. (page 457, para: 3, 4, page 458, para : 4, Sections 2, 3)*
- *length of critical paths: Eberly considers the communication processing over a pivot line and numerical processing increase in execution time (hence, the path length) from the broadcast of the critical combined portion (page 458, para: 4, Sections 2, 3).*

Per claim 13: Eberly further considers selecting/replacing between multiple (1st, 2nd, etc.) pivot line within the matrix (Sections 2, 3).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Garg relating to reordering the elements of a coefficient matrix representing linear simultaneous equations, with the teachings of Eberly relating to accumulative (total) parallel processing time and the length of critical paths, to realize the claimed invention. An obvious motivation exists

since, in this case, the Garg reference teaches to the Eberly reference, and the Eberly reference teaches to the Garg reference. Specifically, both Garg and Eberly teach the reordering of coefficient matrices representing linear equations used in the same technical arena as noted above. Garg teaches to Eberly because Garg discloses that matrix methods have numerous applications including simulation of circuit design and semiconductor modeling (See: Garg CL1-L23). Eberly teaches to Garg because Eberly specifically discloses the use of these matrix methods for improving parallel processing. (See: Eberly) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Garg/Eberly, Abstract/Background) Accordingly, a skilled artisan having access to the teachings of Garg and Eberly, would have knowingly modified the teachings of Garg with the teachings of Eberly (or visa versa) to reduce the development time and cost in realizing the claimed elements of the present invention.

Regarding dependent claims 3, 4, 9, 10, and 14-15: These dependent claims are drawn to the additional steps of reordering (replacing) the matrix elements between combinations of rows and columns based on the symmetry of the coefficient matrix. Garg discloses matrix reordering of row and column selections based on the symmetric properties (positive-definite) of the matrix. (CL1-L20, CL5-L15-27, Fig. 2) Accordingly, as skilled artisan would have knowingly incorporated reordering features based on the symmetric properties of the matrix using the same reasoning as noted above.

Per claim 16: Eberly further considers selecting/replacing between multiple (1st, 2nd, etc.) pivot line within the matrix (Sections 2, 3) and would have knowingly been incorporated by a skilled artisan as previously noted above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 5,655,137 issued to Kevorkian teaches solving simultaneous linear equations using coefficient matrices and parallel processors.

"A New Matrix Solution Technique for General Circuit Simualtin", R. Burch, IEEE Transactions on Computer Aided Design of IC's, vol. 12, No. 2, February 1993, teaches circuit simulation using simultaneous linear equations and coefficient matrices.

"Parallel Programming with Control Abstraction", L.A. Crowl, ACM transactions on Prog. Lang., Vol. 16, No. 3, May 1994, teaches solving simultaneous linear equations using coefficient matrices and parallel processors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

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